

Features

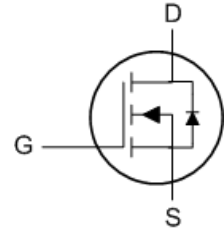
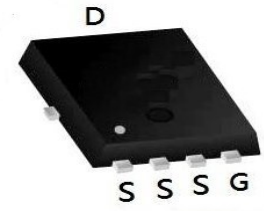
- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$


Product Summary

BVDSS	RDSON	ID
40V	2mΩ	120A

Applications

- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

PDFN5060-8L Pin Configuration

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ C$	Continuous Drain Current ¹	120	A
$I_D@T_C=100^\circ C$	Continuous Drain Current ¹	76	A
I_{DM}	Pulsed Drain Current ²	480	A
EAS	Single Pulse Avalanche Energy ³	180	mJ
I_{AS}	Avalanche Current	30	A
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	65.7	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient (Steady State) ¹	---	60	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	1.9	$^\circ C/W$

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =G50uA	I €	---	---	V
ΔBV _{DSS} /ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =1mA	---	---	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =G€A	---	G	G	mΩ
		V _{GS} =4.5V, I _D =F€A	---	G	H	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	F€	F	G	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	---	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =I €V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =I €V, V _{GS} =0V, T _J =100°C	---	---	F00	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =F€V, I _D =G€A	---	í	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	F	---	Ω
Q _g	Total Gate Charge	V _{DS} =G€V, V _{GS} =F€V, I _D =G€A	---	I G	---	nC
Q _{gs}	Gate-Source Charge		---	í	---	
Q _{gd}	Gate-Drain Charge		---	7.2	---	
T _{d(on)}	Turn-On Delay Time	VGS=10V, VDD=G€V, RG=3Ω, ID=G0A	---	J	---	ns
T _r	Rise Time		---	ì	---	
T _{d(off)}	Turn-Off Delay Time		---	H	---	
T _f	Fall Time		---	F	---	
C _{iss}	Input Capacitance	V _{DS} =G€V, V _{GS} =0V, f=1MHz	---	Ċ	---	pF
C _{oss}	Output Capacitance		---	í	---	
C _{rss}	Reverse Transfer Capacitance		---	G	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,4}	V _G =V _D =0V, Force Current	---	---	120	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =1A, T _J =25°C	---	---	1.2	V
t _{rr}	Reverse Recovery Time	IF=20A, di/dt=100A/μs, T _J =25°C	---	46	---	nS
Q _{rr}	Reverse Recovery Charge		---	18.4	---	nC

Note :

 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.

2.The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%

3.The EAS data shows Max. rating. The test condition is VR=2I ×0, VDD=25V, VGS=10V, L=0.5mH, IAS=30A.

4.The power dissipation is limited by 150°C junction temperature

 5.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

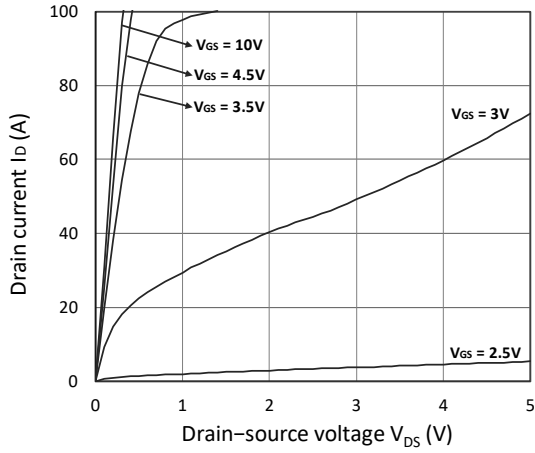
Typical Characteristics


Figure 1. Output Characteristics

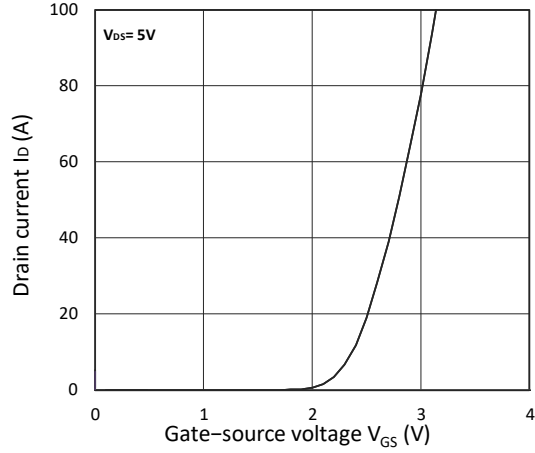


Figure 2. Transfer Characteristics

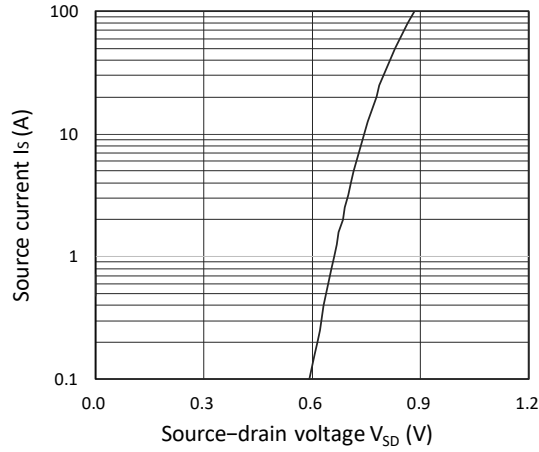
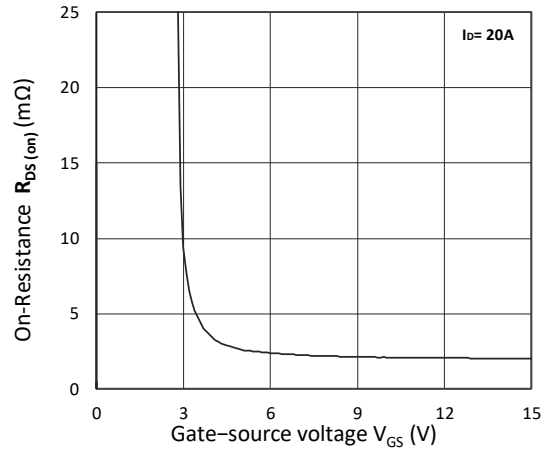
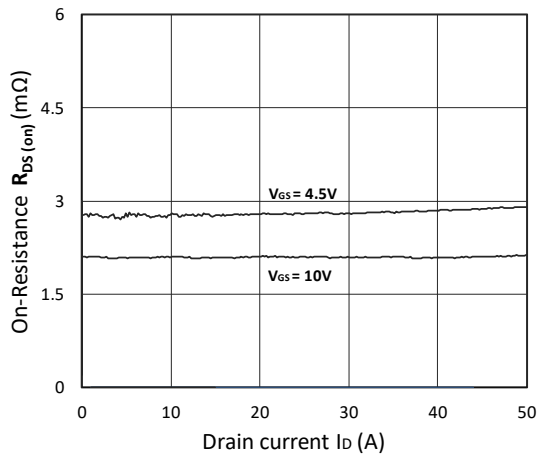
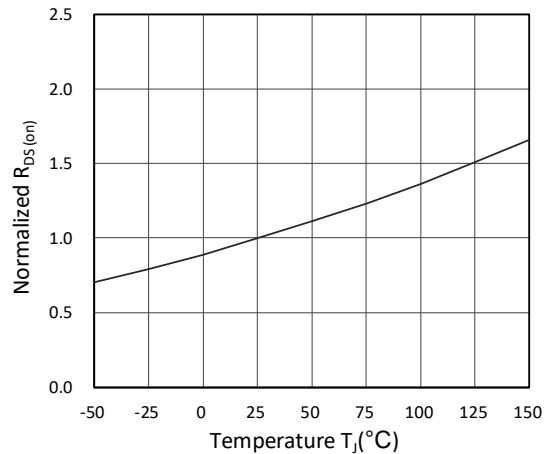


Figure 3. Forward Characteristics of Reverse


 Figure 4. $R_{DS(ON)}$ vs. V_{GS}

 Figure 5. $R_{DS(ON)}$ vs. I_D

 Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

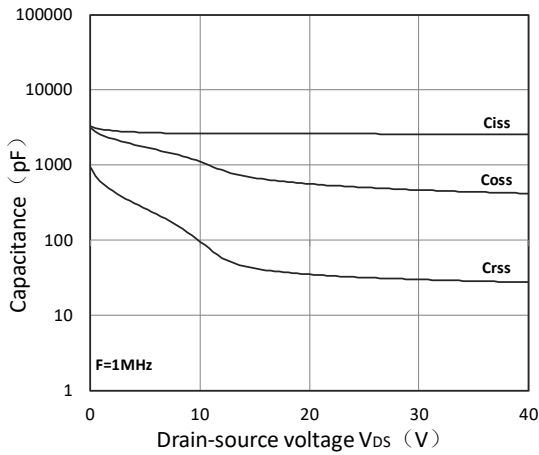


Figure 7. Capacitance Characteristics

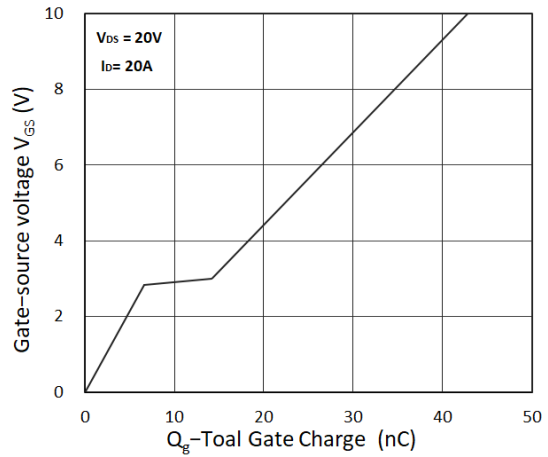


Figure 8. Gate Charge Characteristics

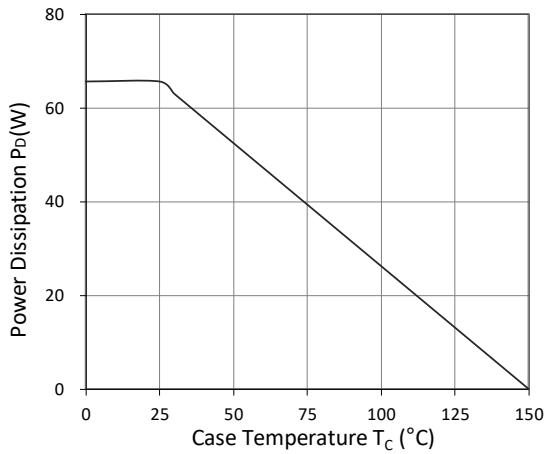


Figure 9. Power Dissipation

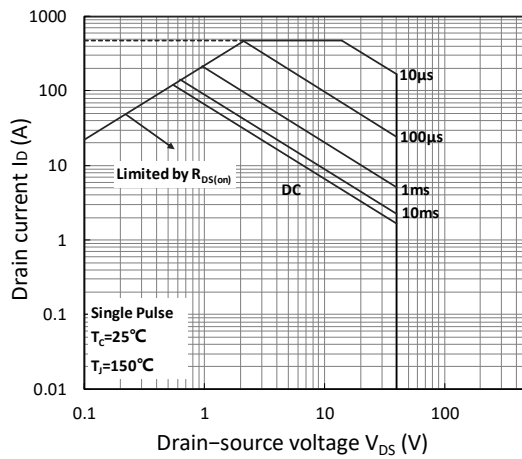


Figure 10. Safe Operating Area

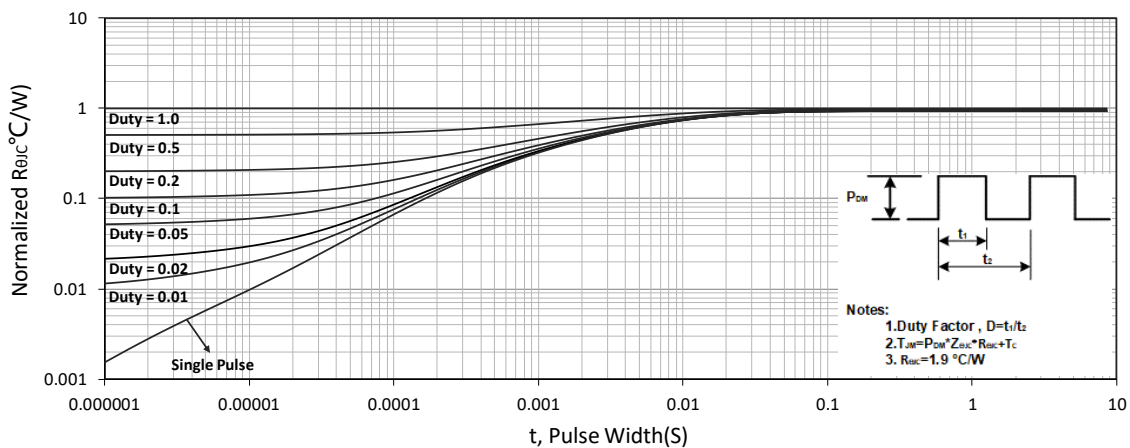


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

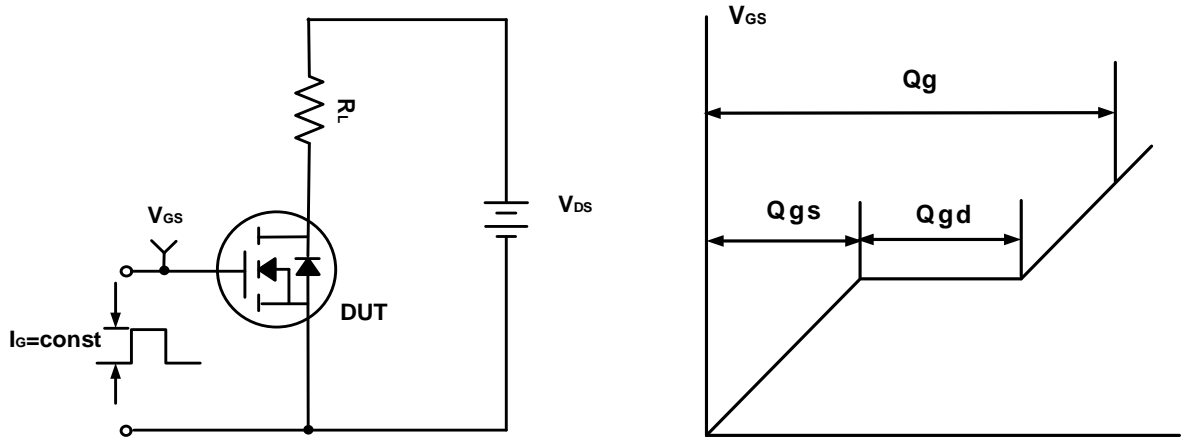


Figure A. Gate Charge Test Circuit & Waveforms

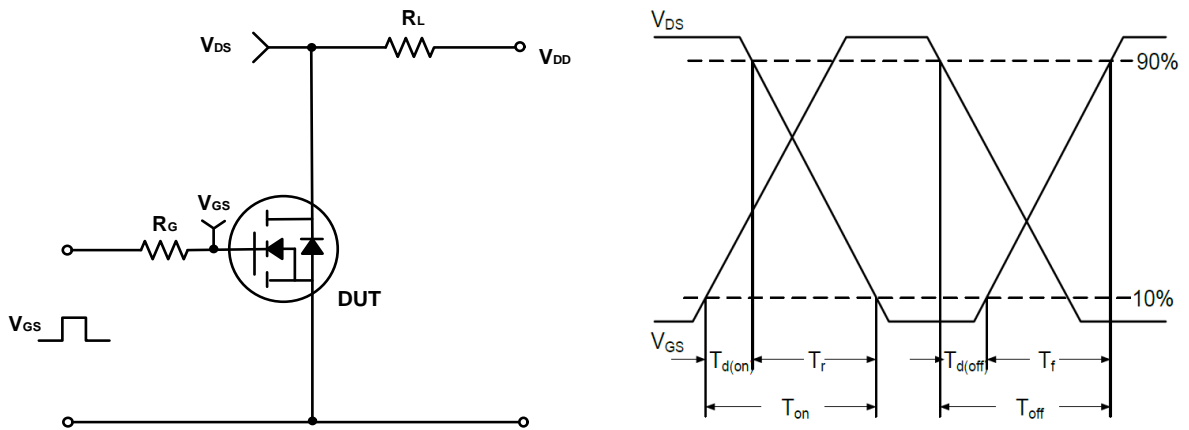


Figure B. Switching Test Circuit & Waveforms

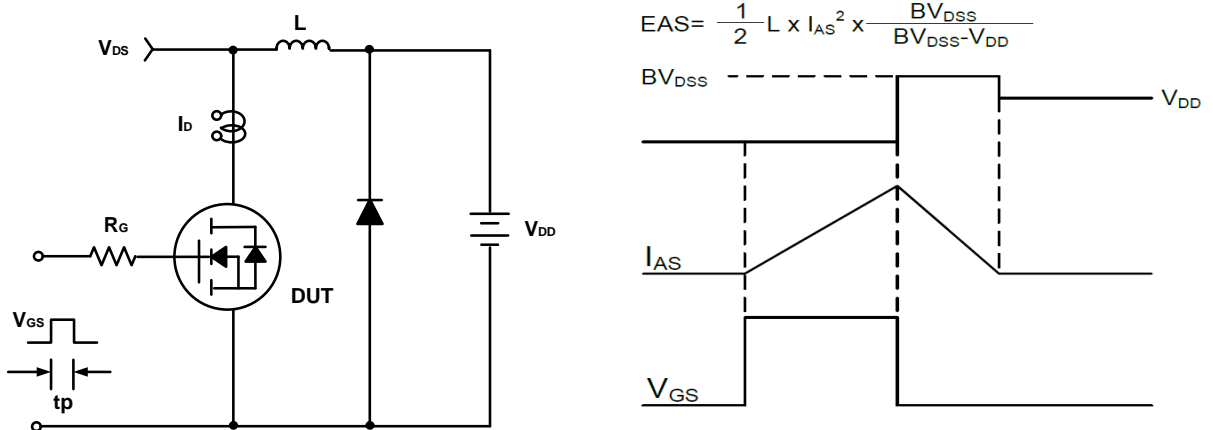
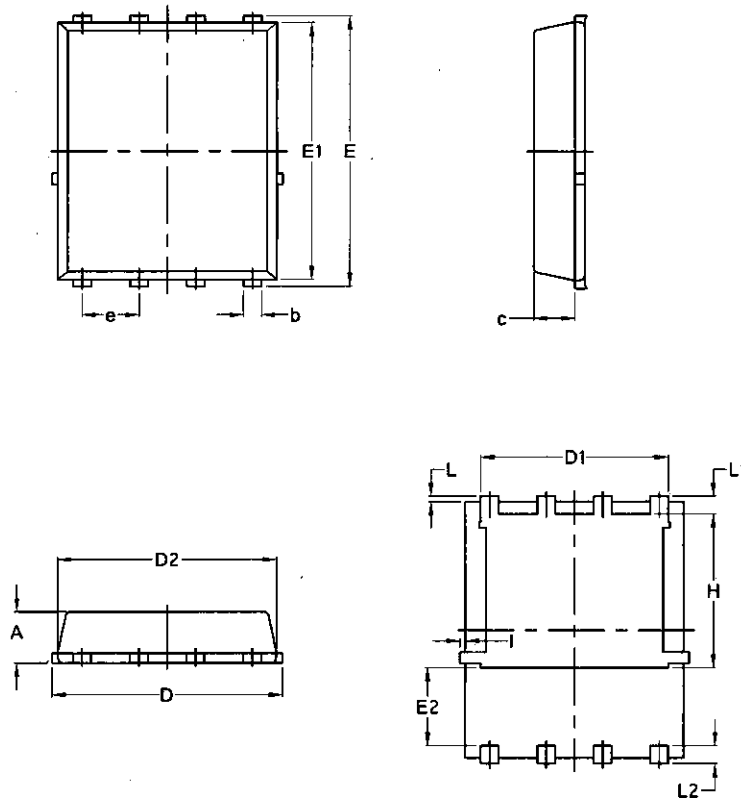


Figure C. Unclamped Inductive Switching Circuit & Waveforms

Package Mechanical Data-PDFN5060-8L- Single


Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070